IN THE CLAIMS:

Please cancel Claims 30-44.

1-26. (Canceled)

27. (Previously Presented) A power semiconductor device made in accordance with the method comprising the steps of:

A. providing a substrate of a first conductivity type;

B. forming a voltage sustaining region on said substrate by:

1. depositing an epitaxial layer on the substrate, said epitaxial layer having a first or a second conductivity type;

2. forming at least one terraced trench in said epitaxial layer, said terraced trench having a trench bottom and a plurality of portions that differ in width to define at least one annular ledge therebetween;

3. depositing a barrier material along the walls and bottom of said trench;

4. implanting a dopant of a conductivity type opposite to the conductivity type of the epitaxial layer through the barrier material lining at said at least one annular ledge and at said trench bottom and into adjacent portions of the epitaxial layer to respectively form at least one annular doped region and another doped region;

5. diffusing the dopant in said at least one annular doped region and said another doped region to cause said at least one annular doped region and said another doped region to overlap one another, whereby a continuous doped column is formed in said epitaxial layer;

6. depositing a filler material in said terraced trench to substantially fill said terraced trench; and

C. forming over said voltage sustaining region at least one region of conductivity type opposite to the conductivity type of the epitaxial layer to define a junction therebetween.

28. (Previously Presented) A power semiconductor device made in accordance with the method of claim 27,

wherein said plurality of portions of the terraced trench are coaxially located with respect to one another, and

wherein said plurality of portions of the terraced trench includes at least three portions that differ in width from one another to define at least two annular ledges and said at least one annular doped region includes at least two annular doped regions, and

wherein the step of forming at least one terraced trench includes the steps of successively etching said at least three portions of the terraced trench beginning with a largest width portion and ending with a smallest width portion.

29. (Previously Presented) A power semiconductor device made in accordance with the method of claim 27,

wherein step (C) further includes the steps of:

forming a gate conductor above a gate dielectric region;

forming first and second body regions in the epitaxial layer to define a drift region therebetween, said body regions having a conductivity type opposite to the conductivity type of the epitaxial layer; and

forming first and second source regions of the first conductivity type in the first and second body regions, respectively.

30-44. (Canceled)